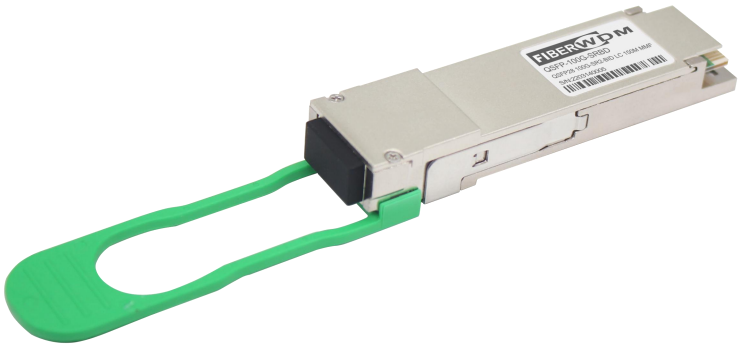
QSFP28-100G-SRBD

QSFP28 Pluggable, Fiber-Optics Module 100Gigabit Ethernet Applications VCSEL PAM4 BiDi 2x50G, MMF Duplex LC Connector



Description

The QSFP-100G-SRBD is a four-channel, pluggable, multimode, fiber-optic QSFP28 transceiver for 100-Gigabit Ethernet applications. This transceiver is a high-performance module for short-range data communication and interconnect applications. It integrates four host electrical data lanes in each direction at 25 Gb/s into two optical lanes at 50 Gb/s giving an aggregated bandwidth of 100 Gb/s. It allows optical communication up to 100m over a two-fiber duplex LC optical multimode OM4 cable. The pull tab facilitates the insertion and extraction of these transceivers in a high-density environment. Each electrical lane operates at 25.78125 Gb/s and conforms to the 100GE CAUI4 interface with the host FEC turned off.

These modules are designed to operate over multimode fiber systems using nominal wavelengths of 850 nm and 900 nm. The electrical interface uses a 38-contact QSFP28-edge type connector. The optical interface uses a conventional two-fiber duplex LC MMF connector. This module incorporates ’s proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Features

- Compliant to 100GbE electrical specification 802.3bm (Annex 83E CAUI-4) with No Host FEC
- 100G link distances up to 70m OM3, 100m OM4 per TIA informative guidance proposal V2, and 150m OM5 per TIA-492AAAE specification.
- 40G link distances up to 75m OM3, 110m OM4 per TIA informative guidance proposal V2, and 160m OM5 per TIA-492AAAE specification.
- QSFP28 MSA specification-compliant, including new functions per SFF-8636
- Class 1 eye safety
- Pull tab: ease of transceiver insertion and extraction
- +10°C to +70°C case temperature operating range
- Dual wavelength VCSEL bi-directional optical interface, PAM4 2 × 50-Gb/s 850 nm/900 nm
- Proven high reliability 850-nm and 900-nm technology: VCSEL transmitter and PIN detector
- Hot pluggable QSFP28 transceiver for ease of installation and servicing
- Two-wire serial (TWS) interface with digital monitoring and maskable interrupts for expanded functionality

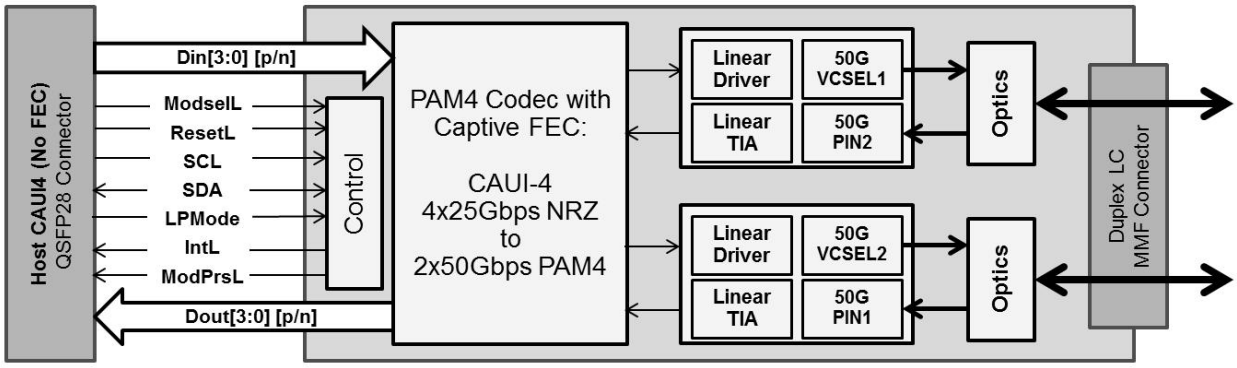
Applications

- 100-Gigabit Ethernet interconnects
- Datacom/telecom switch and router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

QSFP28 Relevant Specifications per SFF-8665

Steering Document	Low Speed, Connector and Electrical Requirements	Common Management Specification/ Memory Map	Form Factor/ Module Mechanical	Cage/Connector Solution	
SFF-8665	SFF-8679	SFF-8636	SFF-8661	SFF-8662 and SFF-8663	Style A
				SFF-8672 and SFF-8683	Style B

Figure 1: Transceiver Block Diagram



Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates a 4 × 25G CAUI4 Annex 83E-compliant electrical input block with Equalization (EQ) block, integrated PAM4 and FEC encoder, laser driver, diagnostic monitors, and control and bias for the dual wavelength Vertical Cavity Surface Emitting Laser (VCSEL) sources. The transmitter is designed for EN 60825 and CDRH Class 1M eye safety compliance. The Tx input buffer provides CAUI4-compliant differential inputs presenting a nominal differential input impedance of 100Ω. AC-coupling capacitors are located inside the QSFP28 module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a two-wire serial (TWS) interface of clock and data signals.

Receiver

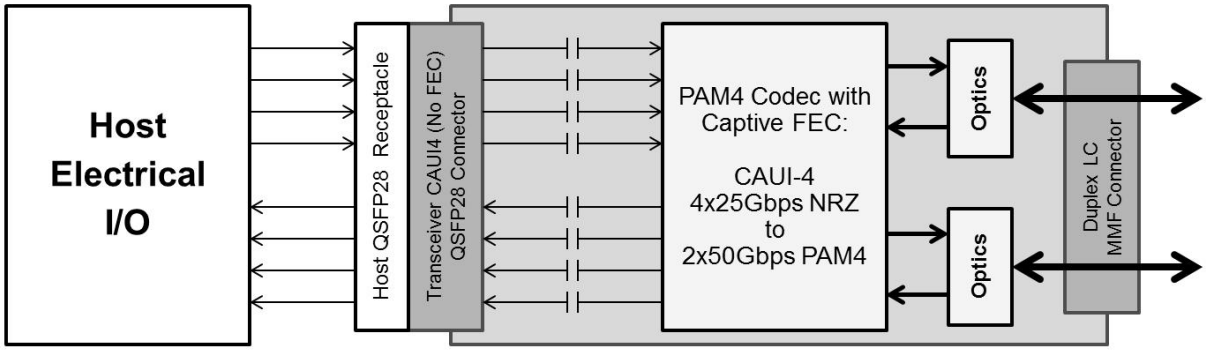
The optical receiver portion of the transceiver (see Figure 1) incorporates dual PIN photodiodes, trans-impedance amplifiers (TIAs), integrated PAM4 and FEC decoder, and 4 × 25G CAUI4 Annex 83E-compliant electrical output blocks. The Rx output buffer provides CAUI4-compliant differential outputs for the high-speed electrical interface presenting nominal single-ended output impedances of 50Ω to AC ground and 100Ω differentially that should be differentially terminated with 100Ω. AC-coupling capacitors are located inside the QSFP28 module and are not required on the host board.

The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through the TWS interface. To reduce the need for polling, a hardware interrupt signal INTL is provided to inform hosts of an assertion of LOS or Tx_FAULT.

High-Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP28 module. The high-speed signal lines are internally AC coupled, and the electrical inputs are internally terminated to 100Ω differential. All transmitter and receiver electrical channels are compliant to module CAUI4 specifications per IEEE 802.3 Annex 83E.

Figure 2: Application Reference Diagram



Control Signal Interface

The module has the following low speed signals forcontrol and status: ModSelL, LPMode, ResetL, ModPrsL, and IntL. In addition, an industry-standard two-wire serial interface is scaled for 3.3V LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in Control Interface and Memory Map.

The registers of the serial interface memory are defined in Control Interface and Memory Map.

Regulatory and Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD, and RoHS. See Regulatory Compliance for details regarding these and component recognition. Note that the transmitter module is a Class 1 laser product.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Wave soldering, reflow soldering, and aqueous wash processes with the modules on board are not recommended. Observe normal handling precautions for electrostatic discharge-sensitive devices.

Each module is supplied with an inserted port plug for the protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber-optic cable, clean the cable end to avoid contamination from the cable plug. The port plug ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard LC port cleaning methods may be used. Use dry nitrogen or clean dry air at less than 20 psi to dislodge the contamination. Liquids are not advised.

Absolute Maximum Ratings

Stress in excess of any of the individual absolute maximum ratings can cause immediate catastrophic damage to the module even if all other parameters are within recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the absolute maximum ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	Ts	–40	85	°C	
3.3V Power Supply Voltage	Vcc	–0.5	3.6	V	
Data Input Voltage – Single Ended		–0.5	Vcc + 0.5	V	
Data Input Voltage – Differential	|VDIp –- VDIn|	—	0.8	V	a
Control Input Voltage	Vi	–0.5	Vcc + 0.5, 3.6	V	
Control Output Current	Io	–20	20	mA	
Relative Humidity	RH	5	95	%	

a. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry (SFF-8679). The damage threshold of the module input shall be at least 1600 mV peak-to-peak differential.

Recommended Operating Conditions[1]

Recommended operating conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the recommended operating conditions, reliability is not implied, and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typ.	Max.	Units	Reference
Case Temperature	Tc	+10	—	+70	°C	a
3.3V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signal Rate per Channel, 100 GbE		10.3125	25.78125	—	GBd	b
Power Supply Noise		—	—	50	mVpp	c
Receiver Differential Data Output Load		—	100	—	Ω	
Fiber Length (OM3)	0.5	—	—	70	m	d
Fiber Length (OM4)	0.5	—	—	100	m	e
Fiber Length (OM5)	0.5	—	—	150	m	f

a. The position of case temperature measurement is shown in Figure 7. Continuous operation at the maximum recommended operating case temperature should be avoided to not degrade reliability.

b. CAUI-4 operation with no host-generated FEC. The QSFP-100G-SRBD must not receive precoded FEC signals from the host ASIC, which will interfere with the captive FEC generated and recovered within the optical transceiver link.

c. Power supply noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 6 for the recommended power supply filter.

d. OM3 fiber effective modal bandwidth is 1948 MHz-km 50-µm MMF (minimum) at 847nm, 1778 MHz-km at 863 nm, 1345 MHz-km at 900 nm, and 1222 MHz-km at 916 nm per the TIA informative guidance proposal V2. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

e. OM4 fiber effective modal bandwidth is 4442 MHz-km 50-µm MMF (minimum) at 847nm, 3643 MHz-km at 863 nm, 2179 MHz-km at 900 nm, and 1878 MHz-km at 916 nm per the TIA informative guidance proposal V2. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

f. OM5 fiber effective modal bandwidth is 4442 MHz-km 50-µm MMF (minimum) at 847 nm, 4353 MHz-km at 863 nm, 3366 MHz-km at 900 nm, and 2939 MHz-km at 916 nm per the TIA-492AAAE specification. The maximum link distance is based on an allocation of 1.5-dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

General Electrical Characteristics[2]

The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Symbols	Min.	Typ.	Max.	Units	Reference
Transceiver Power Consumption		—	—	3.5	W	
Transceiver Power Supply Current		—	—	1130	mA	
AC-Coupling Capacitors (Internal)		—	0.1	—	µF	

Control signals, LVTTL (3.3V) compatible.

1. For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL, and SDA, see Control Interface and Memory Map.

High Speed Electrical Input Characteristics

From CAUI-4, 802.3 Clause 83E, Table 83E-7.

The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
Signaling Rate, Per Lane	TP1	10.3125	25.78125	—	GBd	± 100 ppm
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	900	—	—	mV	
Differential Input Return Loss, Minimum	TP1	—	Eq 83E-5	—	dB	802.3
Differential to Common-Mode Input Return Loss (Minimum)	TP1	—	Eq 83E-6	—	dB	802.3
Differential Termination Mismatch	TP1	—	—	10	%	
Module Stressed Input Test	TP1a	—	83E.3.4.1	—		802.3
Single-ended Voltage Tolerance Range	TP1a	–0.4	—	3.3	V	
DC Common-Mode Output Voltage	TP1	–0.350	—	2.85	V	a

a. DC common mode voltage is generated by the host. The specification includes the effects of ground offset voltage.

Parameter	Value	Units	Notes/Conditions
Module Stressed Input Test			a
Eye Width	0.46	UI	
Applied Peak-to-Peak Sinusoidal Jitter	IEEE 802.3, Table 88-13		
Eye Height	95	mV	

a. The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	10	—	—	mVpp	
LOS Hysteresis		0.5		4	dB	a

a. LOS hysteresis is defined as 20 × Log(LOS Deassert Level / LOS Assert Level).

Module Input Electrical Characteristics

Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board.
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input.
TP1A	Host ASIC transmitter output across the host board and host edge card connector at the output of the host compliance board.
TP2	Optical transmitter output as measured at the end of a 2m to 5m patch cord mated to the optical module.
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board.
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input.
TP5	Input to host ASIC.

Figure 3: IEEE 802.3 CAUI-4 Compliance Points TP1a, TP4a

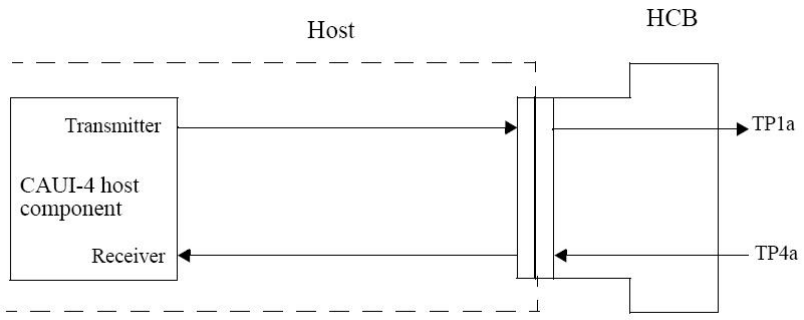


Figure 83E–4—Host CAUI-4 compliance points

NOTE: A reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by the following equation (83E-4) with coefficients given in Table 83E-2.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)}$$

Where:

H(f) is the CTLE transfer function, f is the frequency in GHz

G is the CTLE gain

P1, P2 are the CTLE poles in Grad/s

Z1 is the CTLE zero in Grad/s

j is the square root of –1

f is the frequency in GHz

Reference CTLE Coefficients (Table 83E-2 IEEE 802.3)

Table 1: Table 83E-2

25.78125GBd				
Peaking (dB)	**G**	**P/2 (GHz)**	**P2/2 (GHz)**	**Z1/2 (GHz)**
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

High-Speed Electrical Output Characteristics

From CAUI-4, 802.3 Clause 83E, Table 83E-3.

The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
Signaling Rate, Per Lane	TP4	10.3125	25.78125	—	GBd	± 100 ppm
AC Common-Mode Output Voltage (Max., RMS)	TP4	—	—	17.5	mV, rms	
Differential Output Voltage	TP4	—	—	900	mV	
Eye Width	TP4	0.57	—	—	UI	
Eye Height, Differential	TP4	228	—	—	mV	
Vertical Eye Closure	TP4	—	—	5.5	dB	
Differential Output Return Loss, Min.	TP4	—	Eq 83E-2	—	dB	802.3
Common-to-Differential Mode Conversion Return Loss (Min.)	TP4	—	Eq 83E-3	—	dB	802.3
Differential Termination Mismatch	TP4	—	—	10	%	
Transition Time (20% to 80%)	TP4	12	—	—	ps	
DC Common-Mode Voltage	TP4	–0.35	—	2.85	V	a

a. Capacitively coupled module output is compatible with DC common mode voltage generated by the host. The specification includes the effects of ground offset voltage.

Figure 4: IEEE 802.3 CAUI-4 Compliance Points TP1, TP4

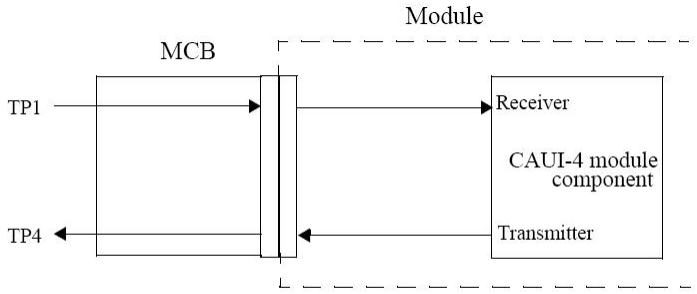


Figure 83E–5—Module CAUI-4 compliance points

High-Speed Optical Transmitter Characteristics

The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
Signaling Rate, Per Lane		10.3125	26.5625	—		± 100 ppm
Center Wavelength 1	TP2	847	855	863	nm	
Center Wavelength 2	TP2	900	908	916	nm	
RMS Spectral Width	TP2	—	—	0.60	nm	a
Average Launch Power, Each Lane	TP2	–6.0	—	+4.0	dBm	
Optical Modulation Amplitude (OMA), Each Lane	TP2	–4.0	—	+3.0	dBm	
OMA – TDECQ, Each Lane	TP2	–5.9	—	—	dBm	
Peak Power, Each Lane	TP2	—	—	+7.0	dBm	
TDECQ, Each Lane	TP2		—	4.9	dB	
Extinction Ratio, Each Lane	TP2	3.0	—	—	dB	
Optical Return Loss Tolerance	TP2	—	—	12	dB	
Encircled Flux	TP2	—	≥ 86% at 19 µm, ≤ 30% at 4.5 µm	—		b
Average Launch Power of OFF Transmitter, Each Lane	TP2	—	—	–30	dBm	

a. RMS spectral width is the standard deviation of the spectrum.

b. If measured into type A1a.2, 50-µm fiber in accordance with IEC61280-1-4.

High-Speed Optical Receiver Characteristics

The following characteristics are defined over the recommended operating conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
Signaling Rate, Per Lane		10.3125	26.5625	—	± 100 ppm	
Center Wavelength 1	TP3	847	855	863	nm	
Center Wavelength 2	TP3	900	908	916	nm	
Damage Threshold	TP3	+7.5	—	—	dBm	a
Receiver Reflectance	TP3	—	—	–15	dB	
Peak Input Power, Each Lane	TP3	—	—	+7.0	dBm	
Optical Modulation Amplitude (OMA), Each Lane	TP3	–5.9	—	+3.0	dBm	
Average Receive Power, Each Lane	TP3	–7.9	—	+4.0	dBm	b
Stressed Receiver Sensitivity in OMA, Each Lane	TP3	—	—	–3.0	dBm	c
Conditions of Stressed Receiver Sensitivity	TP3	—	—	—		d
Stressed Eye Closure (SECQ)	TP3	—	—	4.9	dB	

a. The receiver should be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this inputpower.

b. Average receive power, each lane (minimum) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

c. Measured with conformance test signal at TP3.

d. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/ Conditions
LOS Assert – OMA	TP3	–30	—	—	dBm	
LOS De-Assert – OMA	TP3	—	—	–5.9	dBm	
LOS Hysteresis	TP3	0.5	—	—	dB	

Regulatory Compliance

The QSFP-100G-SRBD complies with all applicable laws and regulations as detailed in the Regulatory Compliance Table. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The QSFP-100G-SRBD is compatible with ESD levels found in typical manufacturing and operating environments as described in the Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a QSFP compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches, and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

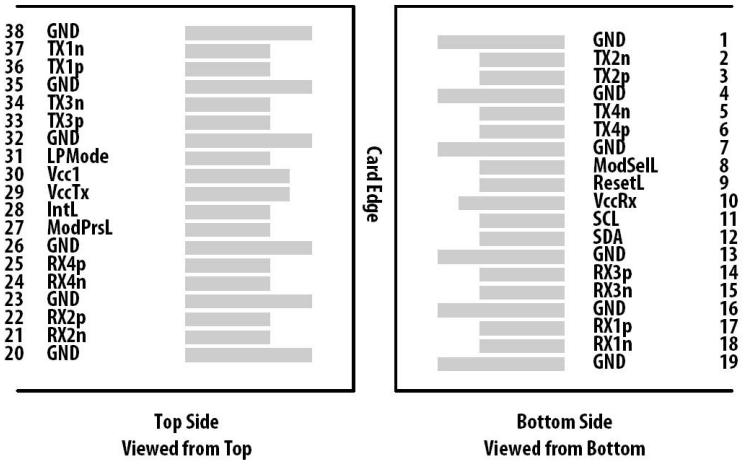
Equipment incorporating multi-gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The QSFP-100G-SRBD compliance to these standards is detailed in the Regulatory Compliance Table. The metal housing and shielded design of the QSFP-100G-SRBD minimizes the EMI challenge facing the equipment designer.

Flammability

The QSFP-100G-SRBD optical transceiver is made of metal and high-strength, heat-resistant, chemical-resistant, and UL94V-0 flame-retardant plastic.

QSFP28 Transceiver Pad Layout

Figure 5: QSFP28 Module Pin Layout



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	a
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	b
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	b
4		GND	Ground	1	a
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	b
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	b
7		GND	Ground	1	a
8	LVTTL-I	ModSelL	Module Select. When held low by the host, the module responds to two-wire serial communication commands.	3	
9	LVTTL-I	ResetL	Module Reset. The ResetL signal is pulled up to Vcc in the QSFP28 module.	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	c
11	LVCMOS-I/O	SCL	Two-Wire Serial Interface Clock. Requires pull-up resistor to 3.3V on the host board.	3	
12	LVCMOS-I/O	SDA	Two-Wire Serial Interface Data. Requires pull-up resistor to 3.3V on the host board.	3	
13		GND	Ground	1	a
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	b
15	CML-O	Rx3n	Receiver Inverted Data Output	3	b
16		GND	Ground	1	a
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	b
18	CML-O	Rx1n	Receiver Inverted Data Output	3	b
19		GND	Ground	1	a

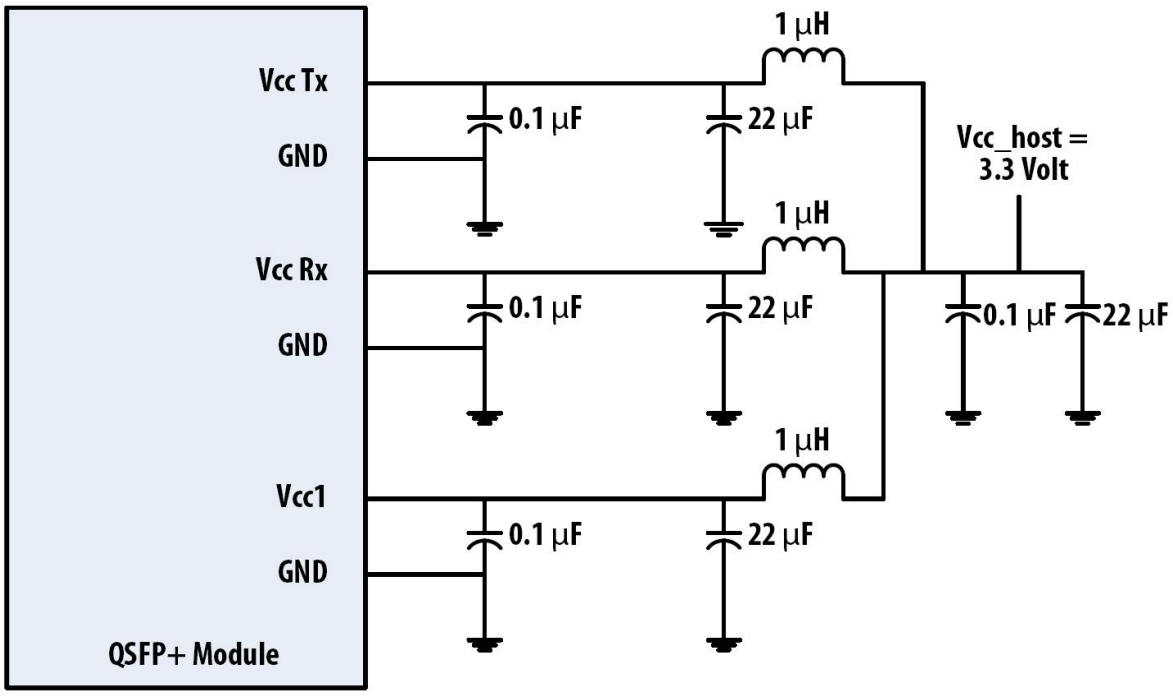
Pin	Logic	Symbol	Description	Plug Sequence	Notes
20		GND	Ground	1	a
21	CML-O	Rx2n	Receiver Inverted Data Output	3	b
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	b
23		GND	Ground	1	a
24	CML-O	Rx4n	Receiver Inverted Data Output	3	b
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	b
26		GND	Ground	1	a
27	LVTTL-O	ModPrsL	Module Present. Requires a pull-up resistor to 3.3V on the host board. Module Present is pulled low in the module.	3	
28	LVTTL-O	IntL	Interrupt. The IntL signal is an open collector output and must be pulled to the host supply voltage (3.3V) on the host board.	3	
29		Vcc Tx	+3.3V Power Supply	2	c
30		Vcc1	+3.3V Power Supply	2	c
31	LVTTL-I	LPMode	Low Power Mode. LPMode is pulled up to Vcc in the module.	3	
32		GND	Ground	1	a
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	b
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	b
35		GND	Ground	1	a
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	b
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	b
38		GND	Ground	1	a

a. GND is the symbol for signal supply (power) common for the QSFP28 module. All are common within the QSFP28 module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

b. For all Tx and Rx high-speed differential inputs/outputs, there are 0.1-μF AC-coupling capacitors are located inside the QSFP28 module and are not required on the host board.

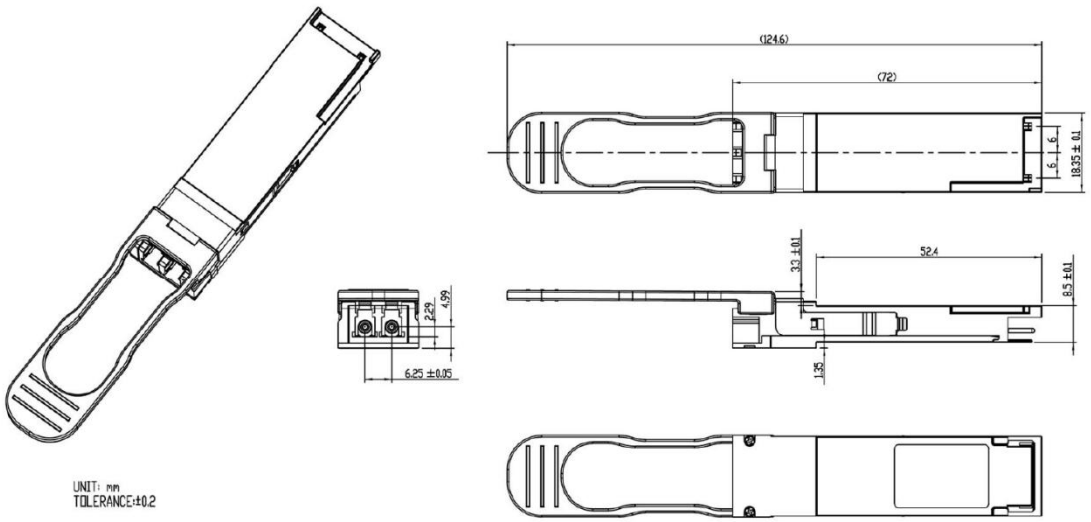
c. Vcc Rx, Vcc1, and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

Figure 6: Recommended Power Supply Filter



Package Outline

Figure 8: Mechanical Package Outline (All Dimensions in mm)



Control Interface and Memory Map

The control interface combines dedicated signal lines for ModSelL, LP Mode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL), and data (SDA) signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3V LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in Control Interface and Memory Map. For more details, refer to QSFP28 SFF-8436.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single two-wire interface bus. When the ModSelL is “High”, the module will not respond to or acknowledge any two-wire interface communication from the host. ModSelL signal input node is biased to the “High” state in the module. To avoid conflicts, the host system should not attempt two-wire interface communications within the ModSelL de-assert time after any QSFP28 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled up to Vcc in the QSFP28 module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init), the host should disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power-up (including hot insertion), the module will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode. LPMode is pulled up to Vcc in the QSFP28 module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set, and High_Power_Class Enable software control bits (Address A0h, byte 93 bits 0, 1, 2), the host controls how much power a module can dissipate.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and de-asserted “High” when the module is physically absent from the host connector.

IntL

IntL is an output signal. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the two-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board.

The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read (refer to SFF-8636).

The user can read the present value of the various diagnostic monitors. Case module temperature, supply voltage, laser bias current for each channel, and receiver input power (Pave) for each channel are reported. All monitor items are 2-byte fields and to maintain coherency, the host must access these with single 2-byte read sequences. For each monitored item, alarm and warning thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault, and monitor flag. ntries in the mask fields are volatile.

Soft Status and Control

A number of soft status signals and controls are available in the QSFP-100G-SRBD transceiver memory and accessible through the TWS interface. Some soft status signals include receiver LOS, transmitter LOS, and diagnostic monitor alarms and warnings. Some soft controls include transmitter disable (Tx_Dis), receiver output disable (Rx_Dis), transmitter squelch disable (Tx_SqDis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. All soft status signals and controls are
per-channel basis. All soft control entries are volatile.

Transmitter LOS

The transmitter LOS status signal is on page 0 address 3 bits 4 to 7 for channels 1 to 4, respectively. Transmitter LOS is based on input differential voltage. This status register is latched, and it is cleared on read.

Receiver LOS

The receiver LOS status signal is on page 0 address 3 bits 0 to 3 for channels 1 to 4, respectively. Receiver LOS is based on the input optical modulation amplitude (OMA). This status register is latched, and it is cleared on read. The first 50G incoming optical lane is mapped into RX lanes 1 and 2 in the memory map, and the second 50G incoming optical lane is mapped into RX lanes 3 and 4.

Transmitter LOL

The transmitter loss of lock status signal is on page 0 address 5 bits 4 to 7 for channels 1 to 4, respectively. The loss of lock flag will assert if an enabled Tx-side CDR is not locked to the input data signal. This status register is latched. and it is cleared on read.

Receiver LOL

The receiver loss of lock status signal is on page 0 address 5 bits 0 to 3 for channels 1 to 4, respectively. The loss of lock flag will assert if an enabled Rx-side CDR is not locked to the input data signal. This status register is latched, and it is cleared on read.

Transmitter Fault

The transmitter fault status signal is on page 0 address 4 bits 0 to 3 for channels 1 to 4, respectively. The transmitter fault condition will flag if the laser output power is too high; that is, approaching eye safety levels. When a fault is triggered, the corresponding transmitter channel output will be disabled. Module reset or toggling of soft transmitter disable (Address 86 decimal) can restore the transmitter channel function unless the fault condition persists. This status register is latched, and it is cleared on read.

Transmitter Disable

The transmitter disable control is on page 0 address 86 bits 0 to 3 for channels 1 to 4, respectively. When each Tx lane is disabled the transmitter optical power should be less than –30 dBm. Because the two 25G electrical lanes are multiplexed into one 50G optical lane, issuing a Tx Disable for any one lane in address 86 bits 0 to 3 will turn off the 50G Tx optical source used.

Receiver Disable

The receiver disable control is on page 3 address 241 bits 4 to 7 for channels 1 to 4, respectively. If the receiver output is disabled, the output differential voltage swing shall be less than 50 mVpp.

Transmitter Squelch Disable

The transmitter squelch disable control is on page 3 address 240 bits 0 to 3 for channels 1 to 4, respectively. QSFP-100G-SRBD transceivers have the transmitter output squelch function enabled as default. If any transmitter output is in the Squelched state, both lasers' output power will be turned off.

Receiver Squelch Disable

The receiver squelch disable control is on page 3 address 240 bits 4 to 7 for channels 1 to 4, respectively. QSFP-100G-SRBD transceivers have the receiver output squelch function enabled as default. If the receiver output is in the Squelched state, the output differential voltage swing should be less than 50 mVpp.

Low-Speed Pin Electrical Specifications

Parameter	Symbol	Min.	Max.	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max) = 3.0 mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	
SCL and SDA	VIL	–0.3	Vcc ×0.3	V	
	VIH	Vcc × 0.7	Vcc + 0.5	V	
LPMode, ResetL and ModSelL	VIL	–0.3	0.8	V	|Iin| ≤ 125 µA for 0V < Vin,Vcc
	VIH	2	Vcc + 0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL = 2.0 mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	
Two-Wire Serial (TWS) Interface Clock Rate		—	400	kHz	

Memory Map

The memory is structured as a single address, multiple page approach. The 7-bit device address on the two-wire interface is 1010000b. The structure of the memory is shown in the following figure. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, for example, interrupt flags and monitors. Less time critical entries, for example, serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP28 memory map, refer to the QSFP28 SFF-8636 Specification.

Figure 9: Memory Map