RQDD-400G-EDR4

400Gbps QSFP-DD EDR4 2KM EML MPO transceiver

1. General description

RQD-400G-EDR4 is a 400 Gbps Quad Small Form Factor Pluggable-Double Density (QSFP-DD) optical transceiver designed for 2km optical communication applications.

2. Features

- IEEE 802.3bs Specification compliant
- QSFP-DD MSA compliant
- 4x106.25 Gbps PAM4 optical interface
- 8x53.125 Gbps PAM4 electrical interface
- I2C interface with integrated DDM
- Up to 2km transmission distance on single mode fiber (SMF) with FEC
- upply voltage: 3.3 V
- Maximum power consumption: 12 W
- MTP/MPO-12 connector
- Operating case temperature: 0 to 70 ° C
- RoHS compliant

3. Applications

- 400G Ethernet
- Datacenter enterprise networking

4. Functional description

The module incorporates 4 parallel channels on 1310 nm center wavelength operating at 100 Gbps per channel. The transmitter path incorporates a quad channel electro-absorption modulated laser (EML) driver together with 4 parallel EMLs. On the receiver path, 4 photodiodes (PDs) are connected with a quad channel transmission impedance amplifier (TIA) to convert the parallel 400 Gbps optical input into 4 channels of parallel 100Gbps PAM4 electrical signals. A digital signal processor (DSP) is used to convert 8 channels of 25 GBaud PAM4 signals into 4 channels of 50 GBaud PAM4 signals and also an 8-channel retimer and forward error corrector (FEC) block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the

transmitting and receiving directions, and the optical interface is compliant to QSFP-DD MSA with MTP/MPO-12 connector.

A single +3.3 V power supply is required to power up this product. As per MSA specifications, the module offers 7 low speed hardware control pins: SCL, SDA, ModSelL, ResetL, LPMode/TxDis, ModPrsL and IntL/RxLOSL. SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3 V on the host side. The pull-up resistor value should be 4.7 kohms to 10 kohms.

ModSelL is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. ResetL is a signal that allows the host to reset the module. A low level on the ResetL signal for longer than the minimum pulse length initiates a complete module reset, returning all user module settings to their default state. LPMode/TxDis is an input signal from the host operating with active high logic. If this pin is “high”, the module enters a low-power state. ModPrsL is used to indicate whether the module is plugged in on the connector, ModPrsL is pulled low when inserted and released to high when it is physically absent from the host connector. IntL/RxLOSL pin is used as interruption. When “Low”, it indicates a possible module operational fault, such as alarm and warning.

5. Absolute maximum ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TS	-40	85	°C	
Operating Case Temperature	TOP	0	70	°C	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

6. Recommended operating conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Case Temperature	TOP	0		70	°C	

Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D			2	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

7. Optical specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125±100 ppm			GBaud	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	Modulated
Average Launch Power, each Lane	P_{AVG}	-2.4		4	dBm	1
Outer Optical Modulation Amplitude (OMA outer), each Lane	P_{OMA}	-0.3		4.2	dBm	2
Launch Power in OMA outer minus TDECQ, each Lane		-1.7			dBm	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	

$RIN_{21.4}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125±100 ppm			GBaud	
Modulation Format		PAM4				
Damage Threshold, each Lane	THd	5			dBm	3
Average Receive Power		-6.4		4.5	dBm	4
Receive Power (OMA outer), each Lane				4.7	dBm	
Receiver Sensitivity (OMA outer), each Lane	SEN			-4.9	dBm	5
Stressed Receiver Sensitivity (OMA outer), each Lane	SRS			-2.4	dBm	6
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-10	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
OMA outer of each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ<1.4 dB, the OMA outer (min) must exceed the minimum value specified here.

3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. Receiver sensitivity (OMA outer), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

6. Measured with conformance test signal for BER=2.4x10^{-4}.

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

8. Electrical specifications

The following electrical characteristics are defined over the recommended operating environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Unit	Note
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625±100 ppm			GBd	
Differential peak-peak Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2017 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2017 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2

Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	

DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each Lane	TP4	26.5625±100 ppm			GBaud	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE802.3-2017Equation(83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE802.3-2017Equation(83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2. Meets BER specified in IEEE 802.3bs 120E.1.1.

3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

9. Digital diagnostic functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Note
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Cover full operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Cover full operating temperature range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-3	3	dB	
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%		
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-3	3	dB	

10.Edge connector and pinout description

The electrical pinout of the QSFP-DD module is shown in Figure 1 below.

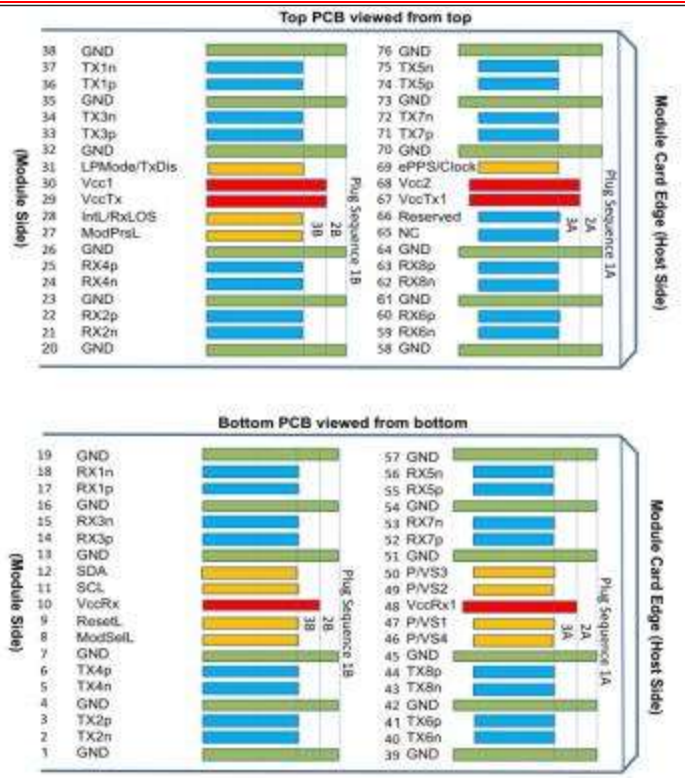

Figure 1. MSA compliant connector.

PIN	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	

13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1

24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	ModPrsL	Module Present	
28	LVTTL-0	IntL/ RxLOS	Interrupt/optional RxLOS	
29		VccTx	+3.3 V Power Supply Transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode/ TxDis	Low Power Mode/Optional TX Disable	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Output	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1

36	CML-I	Tx1p	Transmitter Non-Inverted Data Output	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	
45		GND	Ground	1
46		Reserved	For future use	3

47		VS1	Module Vendor Specific 1	3
48		VccRx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	

60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx 1	+3.3 V Power Supply transmitter	2
68		Vcc2	+3.3 V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply power. All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected theses directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (Not Connect) shall be left unconnected within the module. Vendor

Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

11.Recommended power supply filter

A single +3.3V power supply is required to power up this product.

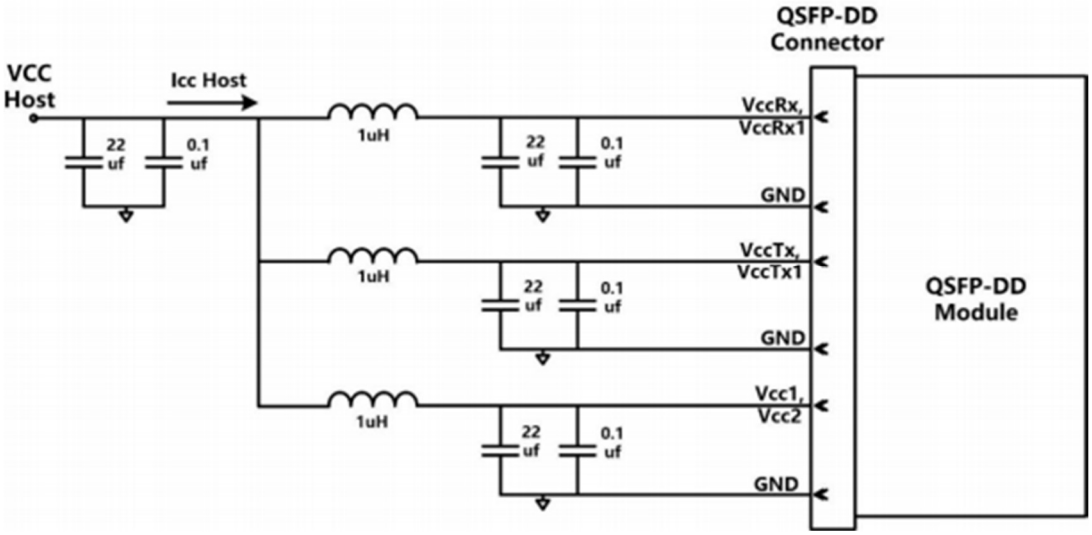

Figure 2. Recommended power supply filter.

12.ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114- A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

13.Laser safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No.50, dated (June 24, 2007).

Caution: use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

14.Transceiver block diagram

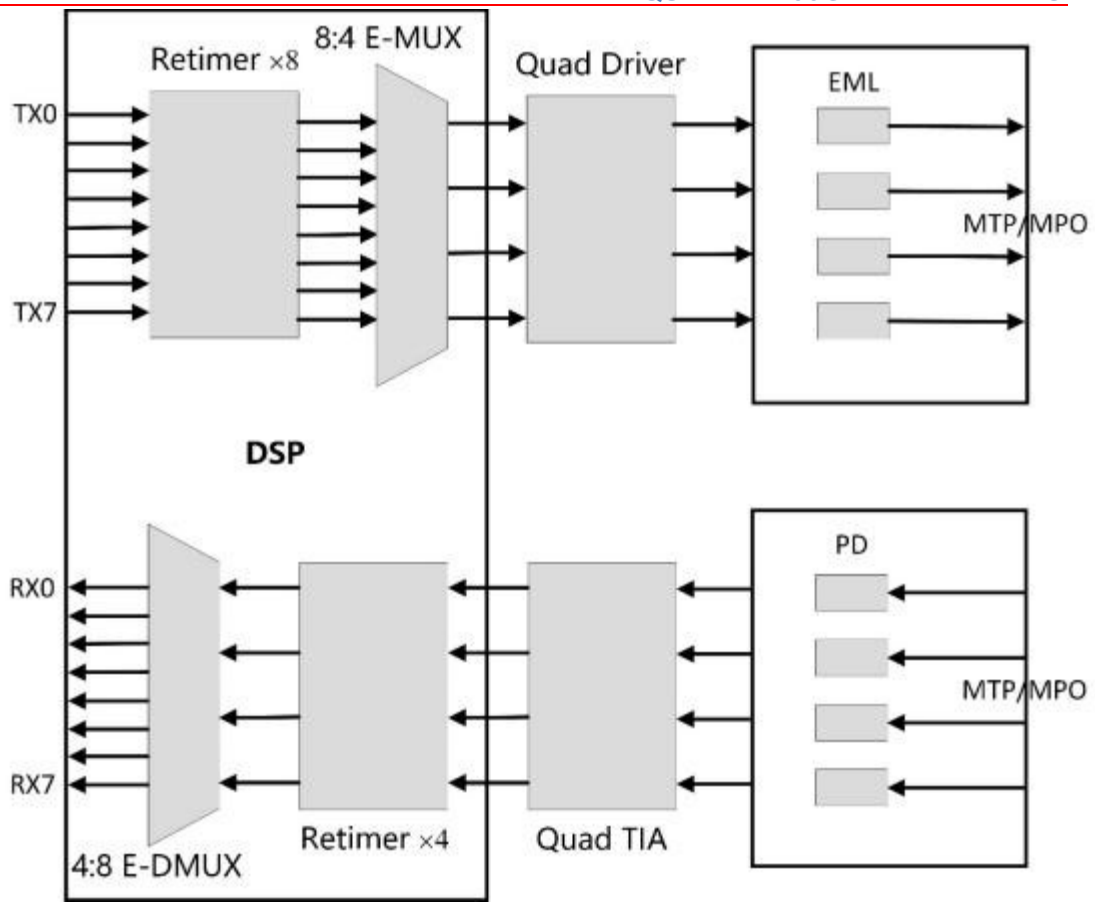

Figure 3. Transceiver block diagram.

15.Mechanical dimensions

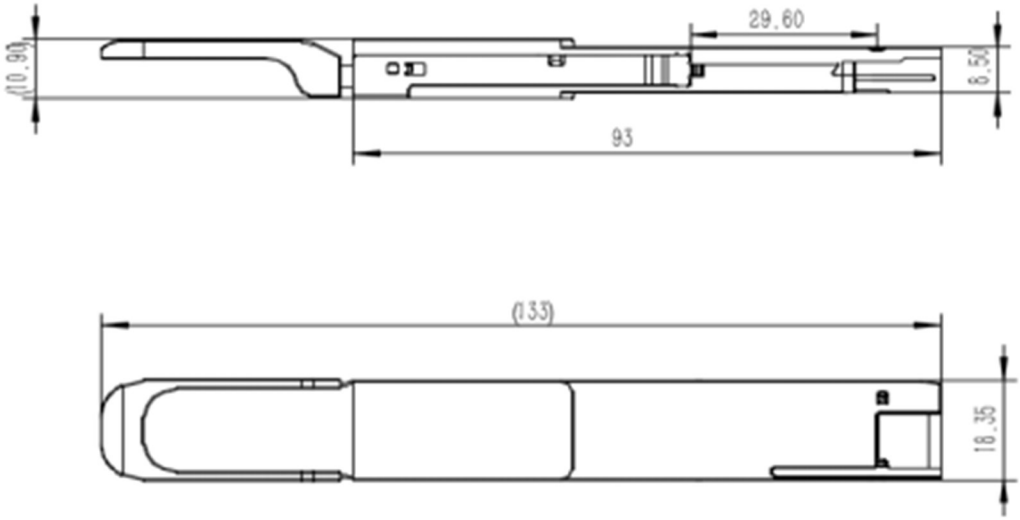

Figure 4. Mechanical outline.

16.Ordering information

Part Number	Product Description
RQDD-400G-EDR4	400G QSFP-DD EDR4 2KMEML MPO

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