RQ-40G-SR4

40G QSFP+ SR4 850nm MPO 100M Transceiver

Features

- 4 independent full-duplex channels
- Up to 10.5Gbps data rate per channel
- MTP/MPO optical connector
- QSFP MSA (SFF-8436) compliant
- Digital diagnostic capabilities
- Capable of over 100m transmission on OM3
- multi-mode fiber
- CML compatible electrical I/O
- Single +3.3V power supply
- Operating case temperature: 0~70C
- XLPPI electric interface (with 1.5W Max power)
- RoHS-6 compliant

Applications

- Data Center
- InfiniBand QDR, DDR and SDR
- 40G Ethernet

Product Description

The module is a parallel 40Gbps Quad Small Form-factor Pluggable (QSFP) optical module. It provides increased port density and total system cost savings. The QSFP full -duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate data rate of 40Gbps over 100 meters of OM3 multi-mode fiber.

An optical fiber cable with an MPO/MTPTM connector can be plugged into the QSFP module receptacle.

The module operates by a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2 -wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information.

The RQ-40G-SR4 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (SFF-8436). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two -wire serial interface.

Ordering information

Part No.	Data Rate	Laser	Fiber Type	Distance*Note1	Optical Interface	Bail Color	Temp. *Note2	DDMI
RQ-40G-SR4	4*10.3Gbps	850nm-VCSEL	MMF	100m	MPO	Beige	ST	Y

Note1: 300m with 50/125μm OM3 MMF

Note2: ST: -5 ~ +70℃

Regulatory Compliance

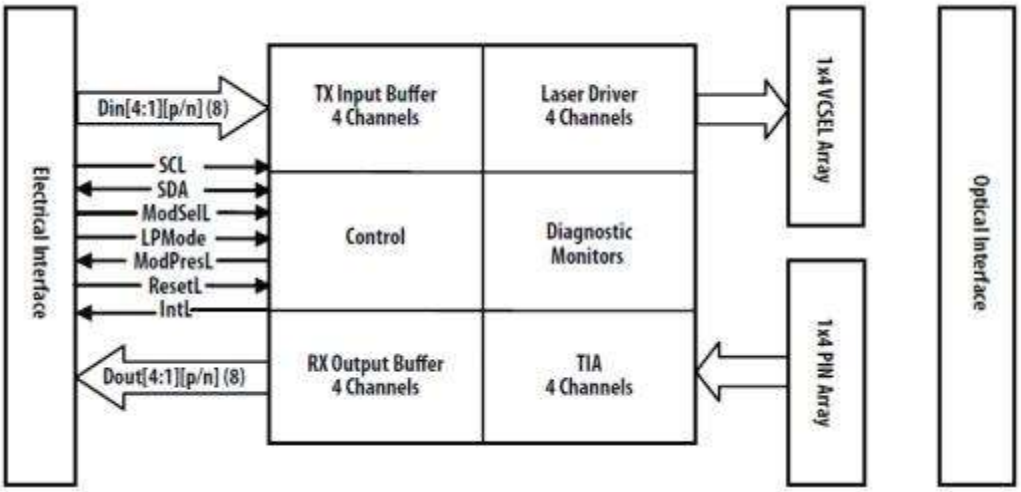
Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883G Method 3015.7	HBM class 1, 1000volts and above, Contact discharge on Golden Finger.
Electrostatic Discharge to the enclosure	IEC-61000-4-2 GR-1089-CORE	Compliant with standards.
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022:2006 VCCI Class B	Compliant with standards Noise frequency range: 30MHz to 18 GHz. System margins depend on customer host board and chassis design.
Immunity	IEC 61000-4-3	Compliant with standards.
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1:2007 EN (IEC) 60825-2:2004+A1	CDRH compliant and Class I laser product.
Component Recognition	UL and CUL EN60950-1:2006	Compliant with standards.
RoHS6	2002/95/EC 4.1&4.2 2005/747/EC 5&7&13	Compliant with standards*note3

Note3:

In light of item 5 in RoHS exemption list of RoHS Directive 2002/95/EC, Item 5: Lead in glass of cathode ray tubes, electronic components and fluorescent tubes.

In light of item 13 in RoHS exemption list of RoHS Directive 2005/747/EC, Item 13: Lead and cadmium in optical and filter glass. The three exemptions are being concerned for FIBERWDM transceivers, because FIBERWDM transceivers use glass, which may contain Pb, for components such as lenses, windows, isolators, and other electronic components.

Block Diagram



Absolute Maximum Ratings*Note4

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-20	85	degC
Relative Humidity (non-condensation)	RH	-	85	%
Supply Voltage	VCC	-0.5	3.6	V
Voltage on LVTTL Input	Vilvttl	-0.5	VCC+0.5	V
LVTTL Output Current	Lolvttl	-	15	mA
Voltage on Open Collector Output	Voco	0	6	V

Note4: Exceeding any one of these values may destroy the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Topc	-5	-	70	C
Power Supply Voltage	VCC	3.1	-	3.5	V
Power Supply Current	ICC	-	-	350	mA
Total Power Consumption (XLPPI)		-	-	1.5	W
Fiber Length: 2000 MHz · km 50μm MMF (OM3)		0.5	-	100	m
Fiber Length: 4700 MHz · km 50μm MMF (OM4)		0.5	-	150	m

Performance Specifications – Electrical

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate, each Lane		-	10.3125	10.5	Gbps	
Power Consumption (XLPPI)		-	-	1.5	W	
Supply Current	ICC	-	0.75	1.0	A	

Control I/O Voltage, High	VIH	2.0	_	VCC	V	
Control I/O Voltage, Low	VIL	0	_	0.7	V	
Inter-Channel Skew	TSK	_	_	150	ps	
Transceiver Power On Initialization Time	Tporinit	-	_	2000	ms	
RESETL Duration			10	_	us	
RESETL De-assert time			_	100	ms	
Power on time			_	100	ms	
Transmitter (XLPPI)						
AC Common mode Voltage Tolerance (RMS)	-	15	-	-	mV	
Tx Input Diff Voltage	VI	90	-	1600	mV	
Tx Input Diff Impedance	ZIN	80	100	120	Ω	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.11			dB	10MHz-11.1GHz
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.1, 0.31, 95, 350			UI	mV
Receiver (XLPPI)						
AC Common mode Voltage Tolerance (RMS)	_	-	-	7.5	mV	
Differential Output Return Loss	See IEEE 802.3ba 86A.4.2.1				dB	10MHz-11.1GHz
Common-mode Output Return Loss	See IEEE 802.3ba 86A.4.2.2				dB	10MHz-11.1GHz
Rx Output Diff Voltage	Vo	-	600	800	mV	
Rx Output Rise and Fall Time	Tr/Tf			35	ps	20% to 80%
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.29, 0.5, 150, 425			UI	mV

Performance Specifications – Optical

Parameter	Symbol	Min	Typ.	Max	Unit
Center Wavelength	λt	840	850	860	nm
RMS Spectral Width	Pm	_ -		0.65	nm
Average Optical Power, each Lane	Pavg	-7.6	_	+1	dBm
Optical Modulation Amplitude (OMA)	Poma	-6	-	+3	dBm
TDP, each Lane		_	_	4	dB

Extinction Ratio	ER	3	-	_	dB
Relative Intensity Noise	Rin	_	_	-128	dB/Hz
Optical Return Loss Tolerance		_	_	12	dB
Transmitter Eye Mask Definition		Complied with IEEE802.3ba			
Average Launch Power OFF Transmitter, each Lane	Poff	-	-	-30	dBm

Receiver

Center Wavelength	Λr	830	850	860	nm
Average Power at Receiver Input, each Lane		-9.5	_	2.4	dBm
Receiver Reflectance		_	_	-12	dB
Los Assert	LosA	-30	_	_	dBm
Los Dessert	LosD	_	_	-14	dBm
Los Hysteresis	LosH	0.5	_	_	dB

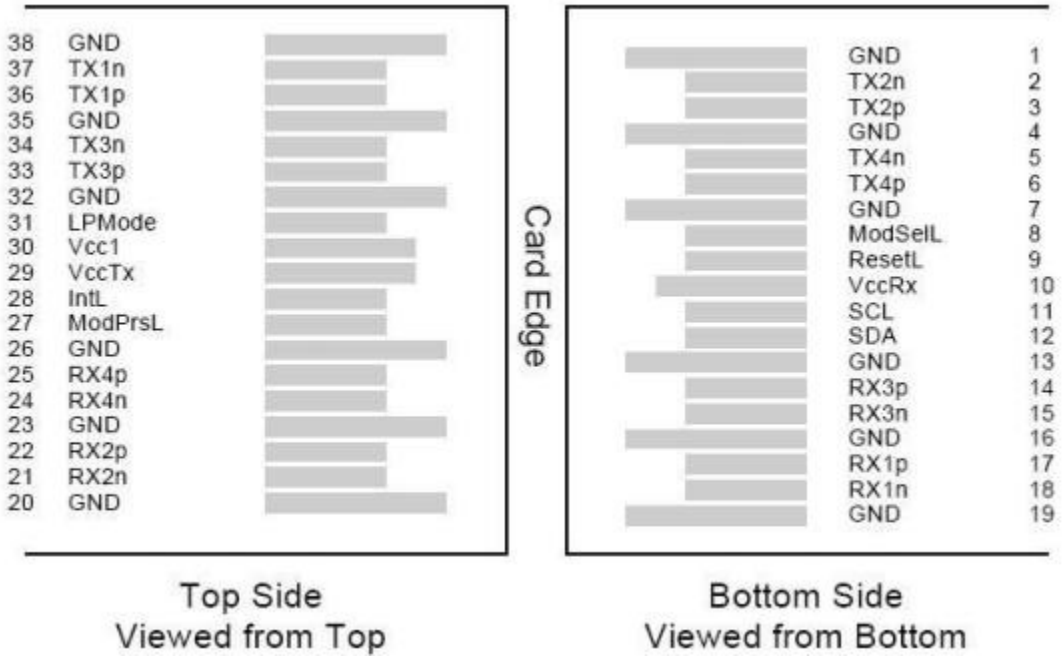
I/O Timing for Control and Status Functions

Parameter	Symbol	Min	Typ.	Max	Unit	Reference
Initialization Time	t_init	_	_	2000	ms	Time from power on, hot plug or rising edge of Reset until the module is fully functional. This time does not apply to non-Power level 0 modules in the Low Power state
LPMode Assert Time	ton_ LPMode	-	-	100	μs	Time from assertion of LPMode until the module power consumption enters power level 1
Interrupt Assert Time	ton_ IntL	_	_	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
Interrupt De-assert Time	Toff_ IntL	_	_	500	μs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for RX LOS, TX Fault and other flag bits
Reset Init Assert Time	t_reset_init	_	_	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Reset Assert Time	t_reset	_	_	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional
Serial Bus Hardware Ready Time	t_serial	_	_	2000	ms	Time from power on until module responds to data transmission over the 2-wire serial bus

Monitor Data Ready Time	t_data	-	-	2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
RX LOS Assert Time	ton_los	-	-	100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted
TX Fault Assert Time	ton_Txfault	-	-	200	ms	Time from TX Fault state to TX fault bit set and IntL asserted
Flag Assert Time	ton_ Flag	-	-	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask	-	-	100	ms	Time from mask bit set until associated IntL assertion is inhibited
Mask Deassert TIme	toff_Mask	-	-	100	ms	Time from mask bit cleared until associated IntL operation resumes
Power Set	ton_Pdow	-	-	100	ms	Time from P_Down bit set until module
Assert Time	n					power consumption enters power level 1
Power Set Deassert Time	toff_ Pdown	-	-	300	ms	Time from P_Down bit cleared until the module is fully functional
RX Squelch Assert Time	ton_ Rxsq	-	-	80	μs	Time from loss of RX input signal until the squelched output condition is reached
RX Squelch Deassert Time	toff_ Rxsq	-	-	80	μs	Time from resumption of RX input signals until normal RX output condition is reached
TX Squelch Assert Time	ton_Txsq	-	-	400	ms	Time from loss of TX input signal until the squelched output condition is reached
TX Squelch Deassert Time	toff_Txsq	-	-	400	ms	Time from resumption of TX input signals until normal TX output condition is reached
TX Disable Assert Time	ton_txdis	-	-	100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal
TX Disable Deassert Time	toff_txdis	-	-	400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal
RX Output Disable Assert Time	ton_rxdis	-	-	100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal
RX Output Disable Deassert Time	toff_rxdis	-	-	100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	-	-	100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled

Squelch Disable Deassert Time	toff_sqdis	-	-	100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality is enabled

Pin Descriptions



Pin Function Definitions

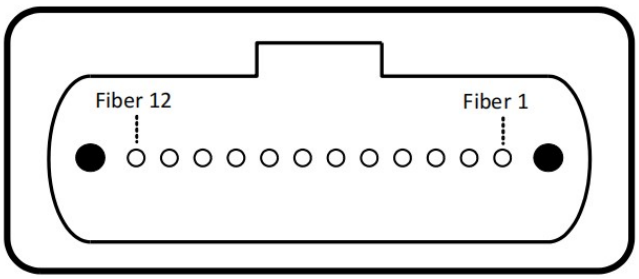
PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

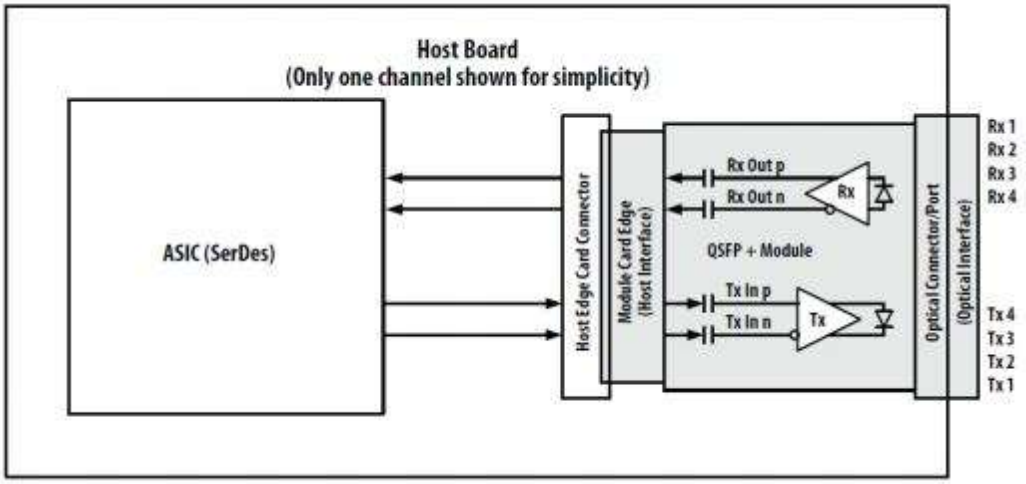
Optical Interface Lanes and Assignment



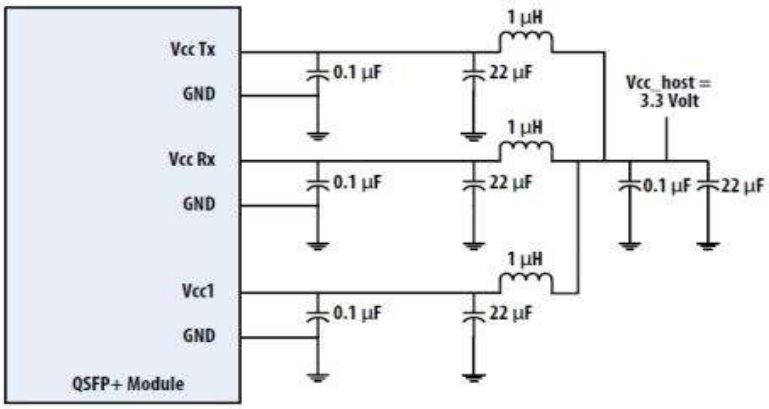
Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3

5	Not used
6	Not used
7	Not used
8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

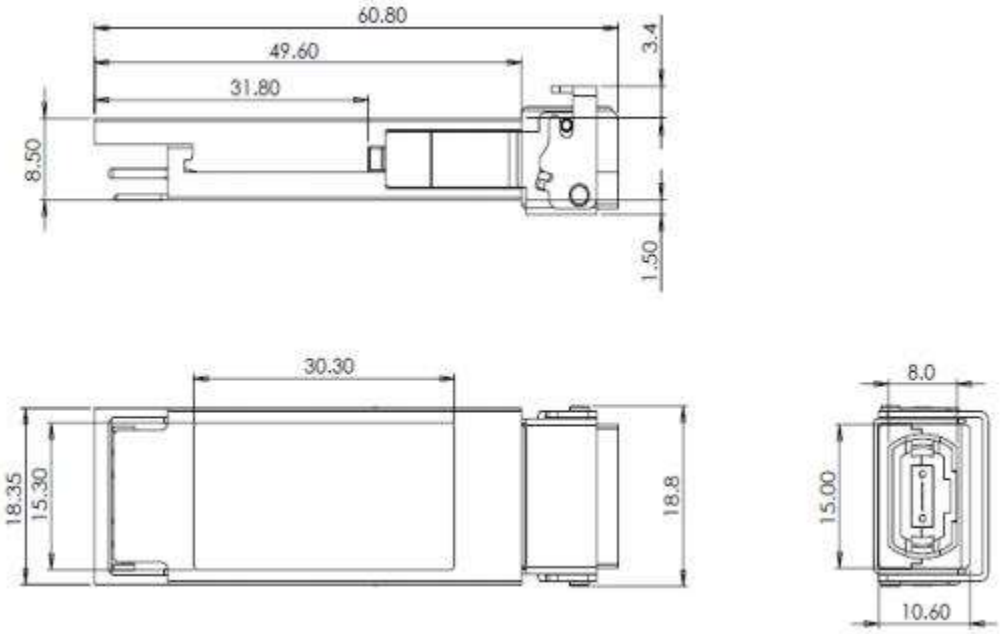
Application Reference Diagram



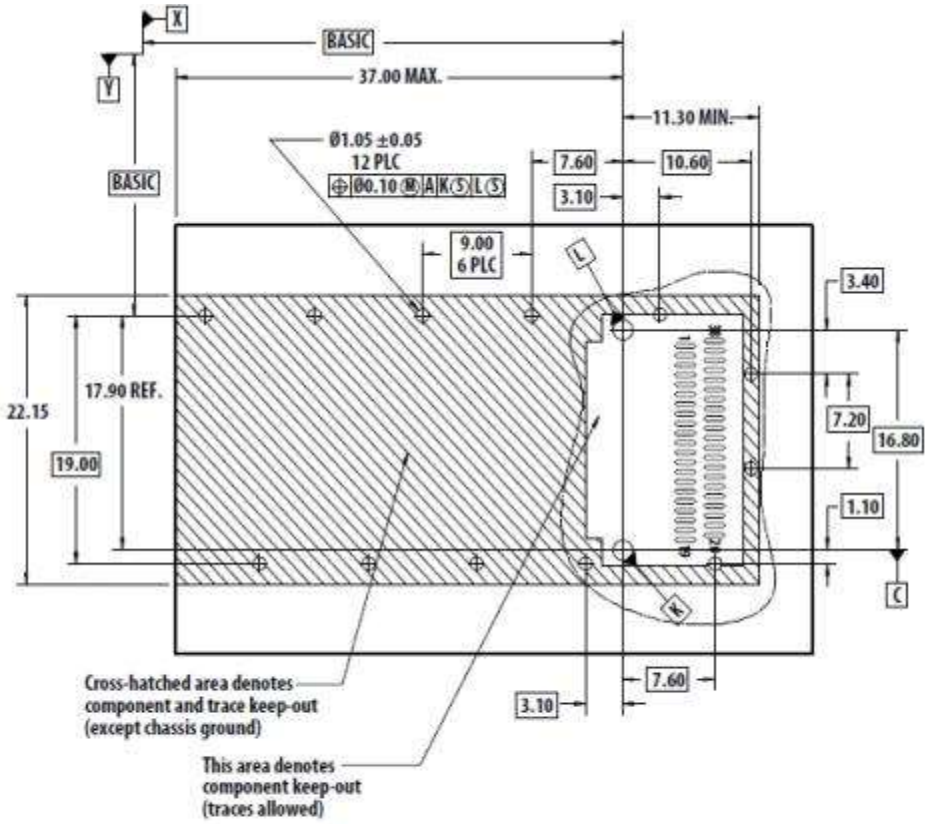
Recommended Host Board Power Supply Circuit



Mechanical Dimension

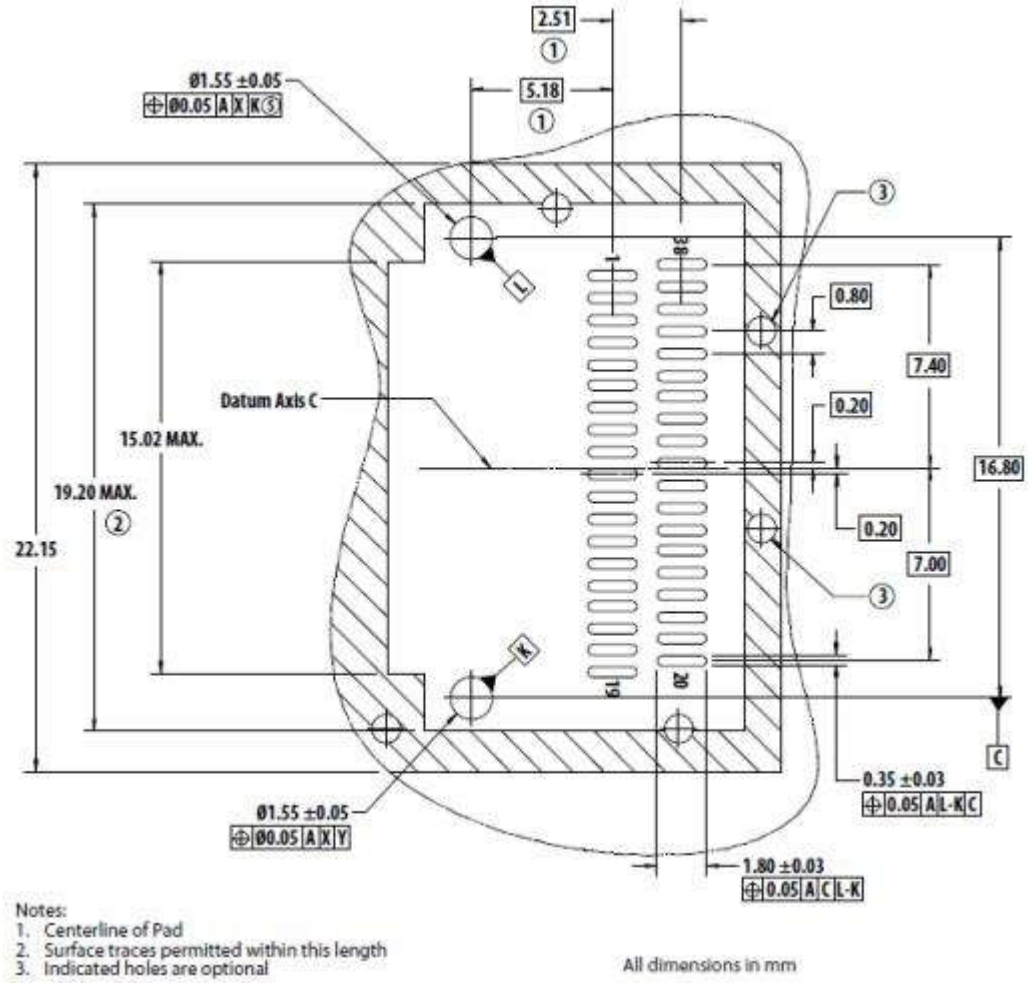


QSFP+ Host Board Mechanical Footprint



Notes:
1. Datum X & Y are established by the customer's fiducial
2. Datum A is the top surface of the host board
3. Location of the edge of PCB is application specific
4. Finished hole size

QSFP+ Host Board Mechanical Footprint Detail



Eye Safety

These transceivers are Class 1 laser products. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the mod ule shall be terminated with an optical connector or with a dust plug.

Notice

FIBERWDM reserves the right to make changes to or discontinue any optical link product or service identified in this publication, without notice, in order to improve design and/or performance.

Applications that are described herein for any of the optical link products are for illustrative purposes only. FIBERWDM makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.